A Miniaturized GaAs Power Amplifier for 1.5 GHz Digital Cellular Phones

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Abstract

An extremely miniaturized GaAs PA has been developed for the application in 1.5-GHz Japanese digital cellular phones. By using MuMIC (i.e. multilayer microwave integrated circuit) technology, the half sized (0.2cc) PA with 1.1W output power has successfully been implemented. The 48-% power-added efficiency has been obtained with drain supply voltage of 3.5-V.

Introduction

In order to miniaturize mobile communication equipments, MMICs are the most effective method to realize the objective. Although several works have been reported on miniaturization, most of them show still large volume and large chip size because of large area occupation of matching circuits 1), 2). To accomplish miniaturization and low cost , we have already reported on the newly developed MuMIC (i.e. multilayer microwave integrated circuit) technology 3), 4). So far reported MuMICs had the low power amplifier application for Japanese personal handy phone systems (PHS) or digital European cordless telecommunications (DECT).

We have successfully developed the high power MuMIC with the output power of over 1W. In this paper, the miniaturized high efficiency GaAs power amplifier for 1.5 GHz digital cellular phones is presented. It is noted that the present MuMIC power amplifier achieves the volume of 0.2cc that is half size of usual one 5). High efficiency and low voltage operation is also achieved at the same time. GaAs power FETs of the δ doped structure contribute to the achievement of the high efficiency operation at the low drain voltage of 3.5V. We consider that the MuMIC technology is the most effective candidate for high frequency circuits.

MuMIC Design

To achieve the small volume and high RF performance of power amplifier, a key point of technology is the adoption of the MuMIC technology. The newly developed high power MuMIC is shown in Fig. 1.

For the high power operation design, the present MuMIC is designed to have a cavity structure for the Aluminum multilayer as shown in Fig. 1. We

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will begin by considering the thermal design of the MuMIC. The thermal design of the high power operation amplifier is worth a mention in passing. The MuMIC thermal model is shown in Fig. 2. The result of the calculation is that the thermal resistance is 15.6℃/W. Junction temperature is estimated to be 44℃ which is obtained from considering the distortion power of 1.1W, the power added efficiencyof 48%, and the power gain of 22dB for the ambient temperature of 25℃ without the duty operation. This result shows that the present cavity type MuMIC is good enough for the high power application.

Matching circuits are formed on the surface of the MuMIC. The λ /4 short stubs providing the drain bias circuits which occupy large circuit area are inserted in the fifth layer of the multilayer structure in order to result in the reduction of the size of the MuMIC. The filter for the second harmonic rejection is inserted in the third layer. These circuits are sandwiched by ground layers. That ends up with high RF separation characteristics.

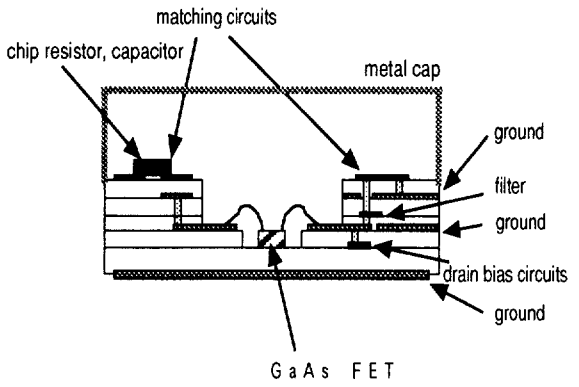
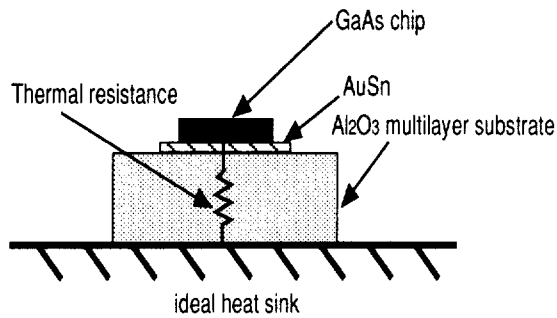


Fig.1. Layer structure of the MuMIC power amplifier.



Thermal resistance (simulated) 14.6 ℃/W

Thermal resistance (measured) 15.6 ℃/W

Fig. 2. Thermal model of MuMIC power amplifier.

FET and Circuit Design

For the purpose of achieving the high efficiency and the low voltage operation of 3.5V, GaAs FET of the δ doped structure is adopted for the power FET 6). In addition, the gate length is designed to be 1μm. The on-resistance is aimed to be lower than 4 Ω /mm. Figure 3 shows the cross-section of designed FETs. The n-GaAs active layer, the i-GaAs layer, and the n^+-GaAs contact layer are provided by selective epitaxial growth.

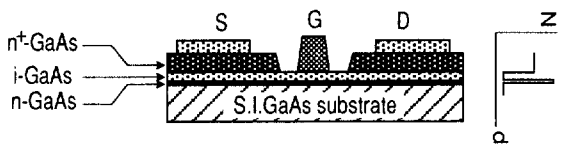


Fig. 3. Cross section of epitaxial power FET.

An equivalent circuit of the power amplifier for 1.5-GHz digital cordless cellular phones is shown in Fig. 4. The two stage amplifier circuit is adopted to achieve the gain of over 20dB. We design the output matching circuit of the second stage to be the optimum IM matching condition. The input matching circuits of the first stage FET is designed to be the optimum gain matching condition. We have arrived at the conclusion that the gate width of the first and the second stage FETs are designed to be 6mm and 18mm, respectively.

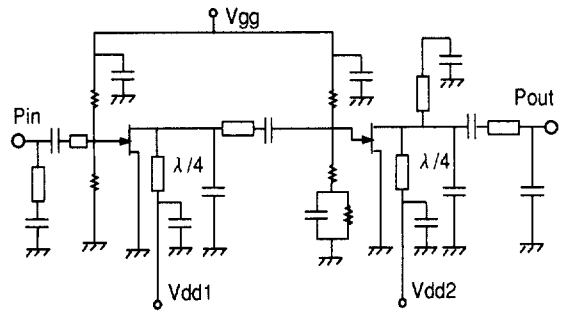


Fig. 4. Equivalent circuit of the GaAs MuMIC power amplifier

Fabrication and RF chracteristics

The photomicrograph of the present GaAs FETs chip is shown in Fig. 5. The size of this chip measures 0.79mm x 2.16mm.

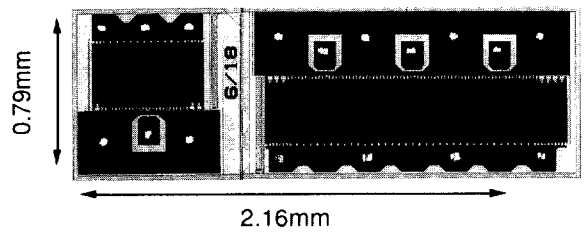


Fig. 5. Photomicrograph of GaAs FET.

The photograph of the implemented MuMIC with mounted GaAs chip is shown in Fig. 6. The MuMIC measures 10mm x 10mm. The RF components such as chip capacitors were also mounted on the surface of the MuMIC. The total volume is achieved to be 0.2cc with a cap.

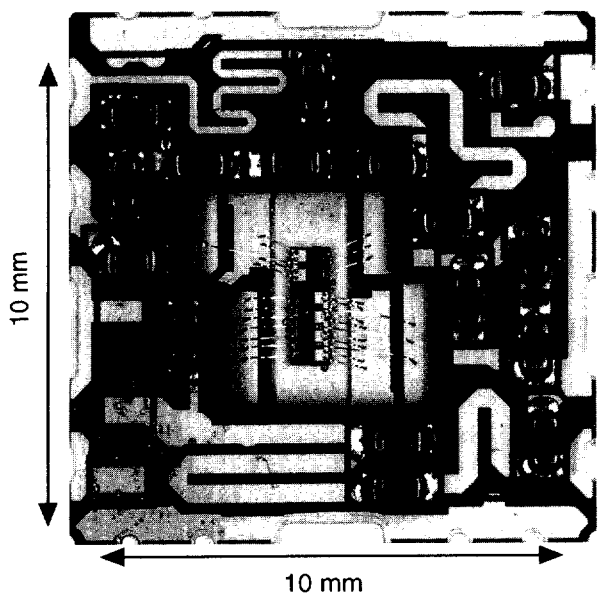


Fig. 6. Top view of MuMIC power amplifier with removing the metal cover.

The input-output characteristics was measured as shown in Fig. 7. No additional matching circuit was used for 50-Ω measurement set-up. The output power was measured to be 1.1W with power-added efficiency of 48% at the drain supply voltage of 3.5-V for 1.44-GHz frequency. The 22-dB gain has been provided with the −51-dBc adjacent channel distortion at ± 50kHz apart from the center frequency for the π/4-shift QPSK modulation.

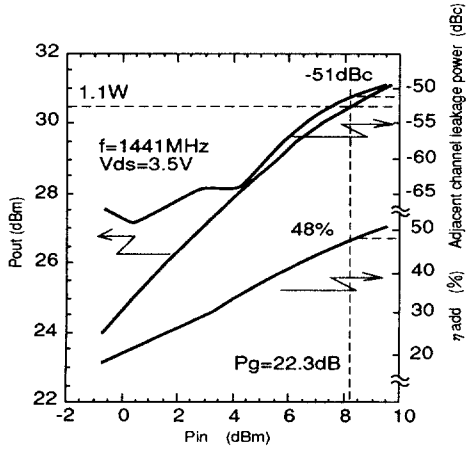


Fig. 7. Measured input-output characteristics of the MuMIC power amplifier.

Conclution

It is shown that the miniaturized high efficiency GaAs MuMIC power amplifier for 1.5GHz digital cellular phones has been developed. The new MuMIC technology have successfully made to reduce the total volume of the high power amplifier to be 0.2cc which is about half size in comparison with the usual one with the output power of over 1W for cellular phone applications. The 48-% efficiency and 22-dB gain at the output power of 1.1W have been obtained with the −51-dBc adjacent channel distortion at ± 50kHz apart from the center frequency for the π/4-shift QPSK modulation at 3.5-V drain supply voltage.

Acknowledgments

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References

1) J. Naber, J. Griffiths, and J. Salvey, "A 1.2 W, 60% Efficient Power Amplifier IC Commercial Applications", IEEE GaAs IC Symposium, pp. 175-178, 1994.

2) K. Mori, et.al., "A UHF Band High Efficiency and High Power Monolithic Amplifier Having Low Drain Bias Voltage", APMC Digest, pp. 663-666, 1994.

3) S. Makioka, et. al., "A High Efficiency GaAs MCM Power Amplifier for 1.9GHz Digital Cordless Telephones", IEEE MMWMC Symp. Digest, pp. 51-54, 1994.

4) N. Yoshikawa, et.al., "Multilayer Microwave Integrated Circuit Technology for GaAs Power Amplifier of Personal Communication System", IEEE ISSCC Digest, pp. 190-191, 1995.

5) K.Tateoka, A.Sugimura, H.Furukawa, M.Yuri. N.Yoshikawa, and K.Kanazawa, "A GaAs MCM Power Amlifier of 3.6V operation with high efficiency of 49% for 0.9GHz Digital Cellular phone systems", IEEE MTT-S Digest, pp. 569-572, 1994.

6) Furukawa, et.al. , "A Novel GaAs Power MESFET with Low Distortion Characteristics Employing Semi-Insulating Setback Layer under the Gate", IEEE Transactions on Electron Devices, (to be published).